High Level Synthesis From Algorithm To Digital Circuit

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High-level synthesis, sometimes referred to as C synthesis, electronic system-level synthesis, algorithmic synthesis, or behavioral synthesis, is an automated design process that interprets an algorithmic description of a desired behavior and creates digital hardware that implements that behavior. Synthesis begins with a high-level specification of the problem, where behavior is generally decoupled from low-level circuit mechanics such as clock-level timing. Early HLS explored a variety of input

High-level synthesis - Wikipedia
High-Level Synthesis: from Algorithm to Digital Circuit should be on each designer ' s and CAD developer ' s shelf, as well as on those of project managers who will soon embrace high level design and synthesis for all aspects of digital system design.

High-level Synthesis: From Algorithm to Digital Circuit ...
This is the goal of high-level synthesis (HLS), and it aims to solve a fundamental problem in system design today. The basic idea is allowing hardware designers to build and verify hardware, with better control over optimization of the design architecture, describing the design at a higher level of abstraction while the tool implements the RTL. It also may be possible to use HLS to improve today ' s algorithms that run on that hardware.

Improving Algorithms With High-Level Synthesis
This book presents an excellent collection of contributions addressing different aspects of high-level synthesis from both industry and academia. High-Level Synthesis: from Algorithm to Digital Circuit should be on each designer ' s and CAD developer ' s shelf, as well as on those of project managers who will soon embrace high level design and synthesis for all aspects of digital system design.

High-Level Synthesis | SpringerLink
Moscow Synthesizer Tool (MOST-SDL) is the enabling technology for our re-engineering process. Synthesis methodology involves using extended Message Sequence Charts to formalize use cases. The input for the synthesis is a set of MSC-92 with states extended with data operations. The synthesis algorithm produces a flexible object-oriented SDL-92 model. The model is syntactically and semantically correct, and complete with respect to the input set of MSCs.

Synthesis Algorithm - an overview | ScienceDirect Topics
High-Level Synthesis Algorithm for the Design of Reconfigurable Constant Multiplier Abstract: Multiplying a signal by a known constant is an essential operation in digital signal processing algorithms. In many application scenarios, an input or output signal is repeatedly multiplied by several predefined constants at different instances.

High-Level Synthesis Algorithm for the Design of ...
The basic operations executed in high-level synthesis are partitioning, scheduling and allocation. Parti- tioning algorithms divide a behavioral description or design structure into subde- scriptions in order to reduce the size of the problem or to satisfy some external constraints.

Scheduling Algorithms for High-Level Synthesis
Abstract - New algorithms for high-level synthesis are presented. The first performs scheduling under hardware resource constraints and improves on commonly used list scheduling techniques by making use of a global priority function.

Scheduling and Binding Algorithms for High-Level Synthesis
The paper presents some scheduling methods in the high-level synthesis. The introduction describes the basics of the high-level synthesis and the role of scheduling. The whole process of the...

(PDF) Scheduling Algorithms in High-Level Synthesis ...
Implement algorithms in ASICs or FPGAs from high levels of abstraction. High-level synthesis is the process of converting a high-abstraction-level description of a design to a register-transfer-level (RTL) description for input to traditional ASIC and FPGA implementation workflows. This high-level design description can be expressed using a variety of methods, depending on the high-level synthesis tool, while the generated RTL is expressed as synthesizable Verilog ® or VHDL ®.

High-Level Synthesis - MATLAB & Simulink
Overview. MATLAB ® is a de facto standard algorithm development tool in many image and signal processing hardware designs. Yet, the traditional path from an abstract floating-point MATLAB model to high-quality RTL code is long and often requires multiple manual coding stages, several designers and many code bases to be maintained.

From MATLAB ® to High-Quality RTL Using High-Level ...
This book presents an excellent collection of contributions addressing different aspects of high-level synthesis from both industry and academia. High-Level Synthesis: from Algorithm to Digital Circuit should be on each designer ' s and CAD developer ' s shelf, as well as on those of project managers who will soon embrace high level design and synthesis for all aspects of digital system design.

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Abstract System designers have started adopting high-level synthesis (HLS) for architectural design because of the higher levels of abstraction offered. The HLS tools provide multiple design choices with tradeoff among different design parameters.